CLAIMS

1. A dynamic logic return-to-zero (RTZ) latching mechanism, comprising:

a complementary pair of evaluation devices responsive to a clock signal;

a dynamic evaluator, coupled between said complementary pair of evaluation devices at a pre-charged node, that evaluates a logic function based on at least one input data signal;

delayed inversion logic that receives said clock signal and that outputs an evaluation complete signal being a delayed and inverted version of said clock signal; and

latching logic, responsive to said evaluation complete signal and the state of said pre-charged node, that asserts the logic state of an output node based on the state of said pre-charged node during an evaluation period between an operative edge of said clock signal and the next edge of said evaluation complete signal, and that returns said output node to zero between evaluation periods.

2. The dynamic logic RTZ latching mechanism of claim 1, wherein said complementary pair of evaluation devices comprises:

a P-channel device having a gate receiving said clock signal and a drain and source coupled between a source voltage and said pre-charged node; and

an N-channel device having a gate receiving said clock signal and a drain and source coupled between said dynamic evaluator and ground.

3. The dynamic logic RTZ latching mechanism of claim 1, wherein said dynamic evaluator comprises a complex logic circuit.

4. The dynamic logic RTZ latching mechanism of claim 1, wherein said delayed inversion logic comprises a series chain of inverters.

5. The dynamic logic RTZ latching mechanism of claim 1, wherein said latching logic comprises:

an N-channel pass device having a gate receiving said evaluation complete signal and a drain and source coupled between said pre-charged node and a pull-up control node;

a first P-channel pull-up device having a gate receiving said evaluation complete signal and a drain and source coupled between a source voltage and said pull-up control node;

a second P-channel pull-up device having a gate coupled to said pull-up control node and a drain and source coupled between said source voltage and said output node; and

an N-channel pull-down device having a gate coupled to said pull-up control node and a drain and source coupled between said output node and ground.

6. The dynamic logic RTZ latching mechanism of claim 5, further comprising added logic coupled between said source voltage and said second P-channel pull-up device and added complementary logic coupled between said output node and ground, said added logic and said added complementary logic collectively operative to prevent a selected state of said output node.

7. The dynamic logic RTZ latching mechanism of claim 1, further comprising a footless latching domino circuit having an input coupled to said output node and a registered output node providing a registered output signal.

8. The dynamic logic RTZ latching mechanism of claim 7, wherein said footless latching domino circuit comprises:

a first P-channel device having a gate receiving said clock signal and a drain and source coupled between a source voltage and a control node;

a first N-channel device having a gate coupled to said output node and a drain and source coupled between said control node and ground;

a first keeper circuit coupled to said control node;

a second P-channel device having a gate coupled to said control node and a drain and source coupled between said source voltage and said registered output node;

a second keeper circuit coupled to said registered output node;

a second N-channel device having a gate receiving said clock signal and a drain and source coupled between said registered output node and an intermediate node; and

a third N-channel device having a gate coupled to said control node and a drain and source coupled between said intermediate node and ground.

9. A dynamic latch circuit, comprising:

a dynamic circuit that pre-charges at least one pre-charged node while a clock signal is low and that evaluates a logic function for controlling the state of said at least one pre-charged node when said clock signal goes high;

a delayed inverter receiving said clock signal and providing an inverted delayed clock signal; and

a latching circuit, coupled to said dynamic circuit and said delayed inverter, that controls the state of an output node based on the state of said at least one pre-charged node during each evaluation period beginning when said clock signal goes high and ending when said inverted delayed clock signal next goes low, and that otherwise asserts said output node to a zero logic state.

10. The dynamic latch circuit of claim 9, wherein said dynamic circuit comprises:

a pull-up device, coupled to a first pre-charged node, that pre-charges said first pre-charged node while said clock signal is low;

a logic circuit, coupled to said first pre-charged node, that evaluates said logic function; and

a pull-down device, coupled to said logic circuit, that enables said logic circuit to evaluate said logic function when said clock signal goes high.

11. The dynamic latch circuit of claim 9, wherein said latching circuit comprises:

a pass device that couples a second node to said at least one pre-charged node when said inverted delayed clock signal is high;

a first pull-up device that pulls said second node high while said inverted delayed clock signal is low;

a second pull-up device that pulls said output node high when said second node is low; and

a pull-down device that pulls said output node low when said second node is high.

12. The dynamic latch circuit of claim 9, wherein said delayed inverter comprises a series chain of inverters.

13. The dynamic latch circuit of claim 9, further comprising a footless latching domino circuit coupled to said output node that provides a corresponding registered output.

14. The dynamic latch circuit of claim 9, further comprising:

said dynamic circuit comprising a plurality of dynamic circuits, each receiving a corresponding one of a plurality of input signals and pre-charging a corresponding one of a plurality of pre-charged nodes; and

said latching circuit comprising a plurality of latching circuits, each coupled to a corresponding one of said plurality of dynamic circuits, each receiving a corresponding one of said plurality of input signals, and each having an output that is wire-ORed coupled to said output node.

15. The dynamic latch circuit of claim 14, wherein each of said plurality of dynamic circuits comprises:

a first P-channel device having a gate receiving said clock signal and a drain and source coupled between a source voltage and a corresponding one of said plurality of pre-charged nodes;

a first N-channel device having a gate receiving a corresponding one of said plurality of input signals and a drain and source coupled between said corresponding pre-charged node and a corresponding one of a plurality of first intermediate nodes; and

a second N-channel device having a gate receiving said clock signal and a drain and source coupled between said corresponding first intermediate node and ground.

16. The dynamic latch circuit of claim 15, wherein each of said plurality of latching circuits comprises:

a third N-channel device having a gate receiving said inverted delayed clock signal and a drain and source coupled between a corresponding one of said plurality of pre-charged nodes and a corresponding one of a plurality of pull-up control nodes;

a second P-channel device having a gate receiving said inverted delayed clock signal and a drain and source coupled between said source voltage and said corresponding pull-up control node;

a third P-channel device having a gate receiving a corresponding one of said plurality of input signals and a drain and source coupled between said source voltage and a corresponding one of a plurality of second intermediate nodes;

a fourth P-channel device having a gate coupled to said corresponding pre-charged node and a drain and source coupled between said corresponding second intermediate node and said output node;

a fourth N-channel device having a gate coupled to said corresponding pre-charged node and a drain and source coupled in a first stack configuration between said output node and ground; and

a fifth N-channel device having a gate receiving said corresponding input signal and a drain and source coupled in a second stack configuration between said output node and ground.

17. The dynamic latch circuit of claim 16, wherein said logic function comprises an exclusive-OR logic function.

18. A dynamic logic RTZ latching method, comprising:

pre-setting a first node while a clock signal is in a first logic state;

dynamically evaluating a logic function to control the logic state of the first node when the clock signal transitions to a second logic state;

delaying and inverting the clock signal and providing a delayed inverted clock signal;

latching a logic state of an output node based on the logic state of the first node determined during an evaluation period beginning when the clock signal transitions to the second logic state and ending with the next corresponding transition of the delayed inverted clock signal; and

returning the logic state of the output node to a low logic state between evaluation periods.

19. The method of claim 18, wherein said pre-setting a first node comprises pre-charging the first node to a high logic state.

20. The method of claim 18, further comprising adding a latching domino circuit to the output node to provide a registered output signal.

21. The method of claim 18, the first logic state being a low logic state and the second logic state being a high logic state, wherein said latching a logic state of an output node comprises:

passing a logic state of the first node to a pull-up control node while the delayed inverted clock signal is in a high logic state;

pulling the output node to a high logic state if the pull-up control node is in a low logic state; and

pulling the output node to a low logic state if the first node is in a high logic state.

22. The method of claim 21, wherein said returning the logic state of the output node to a low logic state comprises keeping the pull-up control node at a high logic state while the delayed inverted clock signal is at a low logic state and also while the clock signal is at a low logic state.